

# 512Mb I-die Mobile SDR SDRAM

16Mb x32, 90FBGA with Lead-Free & Halogen-Free  
(VDD / VDDQ = 1.8V / 1.8V)

## datasheet

SAMSUNG ELECTRONICS RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE.

Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind.

This document and all information discussed herein remain the sole and exclusive property of Samsung Electronics. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or otherwise.

Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

For updates or additional information about Samsung products, contact your nearest Samsung office.

All brand names, trademarks and registered trademarks belong to their respective owners.

© 2009 Samsung Electronics Co., Ltd. All rights reserved.

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Editor</u>
0.0	-First version for target specification.	Nov. 23, 2009	Target	J.Y.Bae
1.0	- Final Datasheet. - Revised DC characteristics. 1. ICC1 : 70/60 -> 65/60 @ 166Mhz, 133Mhz [mA] 2. ICC2NS : 1/1 -> 5/4 @ 166Mhz, 133Mhz [mA] 3. ICC3P : 5/5 -> 3/3 @ 166Mhz, 133Mhz [mA] 4. ICC3N : 20/15 -> 12/12 @ 166Mhz, 133Mhz [mA] 5. ICC3NS : 10/8 -> 8/8 @ 166Mhz, 133Mhz [mA] 6. ICC4 : 80/70 -> 65/60 @ 166Mhz, 133Mhz [mA] 7. ICC5 : 80/80 -> 70/70 @ 166Mhz, 133Mhz [mA]	Dec. 18, 2009	Final	J.Y.Bae

## [Table Of Contents](#)

### **512Mb I-die Mobile SDR SDRAM**

1.0 FEATURES.....	4
2.0 GENERAL DESCRIPTION .....	4
3.0 ORDERING INFORMATION .....	4
4.0 ADDRESS CONFIGURATION .....	4
5.0 FUNCTIONAL BLOCK DIAGRAM .....	5
6.0 PACKAGE DIMENSION AND PIN CONFIGURATION .....	6
7.0 ABSOLUTE MAXIMUM RATINGS .....	7
8.0 DC OPERATING CONDITIONS .....	7
9.0 CAPACITANCE .....	7
10.0 DC CHARACTERISTICS .....	8
11.0 AC OPERATING TEST CONDITIONS .....	9
12.0 OPERATING AC PARAMETER .....	10
13.0 AC CHARACTERISTICS .....	11
14.0 SIMPLIFIED TRUTH TABLE .....	12
15.0 MODE REGISTER FIELD TABLE TO PROGRAM MODES .....	13
15.1 Register Programmed with Normal MRS .....	13
15.2 Normal MRS Mode .....	13
15.3 Register Programmed with Extended MRS .....	13
15.4 EMRS for PASR(Partial Array Self Ref.) & DS(Driver Strength) .....	13
15.4.1 Partial Array Self Refresh .....	14
15.4.2 Internal Temperature Compensated Self Refresh (TCSR) .....	14
16.0 POWER UP SEQUENCE .....	14
17.0 BURST SEQUENCE .....	15
17.1 BURST LENGTH = 4 .....	15
17.2 BURST LENGTH = 8 .....	15

## 4M x 32Bit x 4 Banks Mobile SDR SDRAM in 90FBGA

# 1.0 FEATURES

- VDD/VDDQ = 1.8V/1.8V
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - CAS latency (2 & 3).
  - Burst length (1, 2, 4, 8 & Full page).
  - Burst type (Sequential & Interleave).
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- Special Function Support.
  - PASR (Partial Array Self Refresh).
  - Internal TCSR (Temperature Compensated Self Refresh)
  - DS (Driver Strength)
- DQM for masking.
- Auto refresh.
- 64ms refresh period (8K cycle).
- Extended Temperature Operation (-25°C ~ 85°C).
- Commercial Temperature Operation (-25°C ~ 70°C).
- 90Balls FBGA( -SXXX -Pb, -DXXX -Pb Free).

# 2.0 GENERAL DESCRIPTION

The K4M51323PI is 536,870,912 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 32 bits, fabricated with SAM-SUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

# 3.0 ORDERING INFORMATION

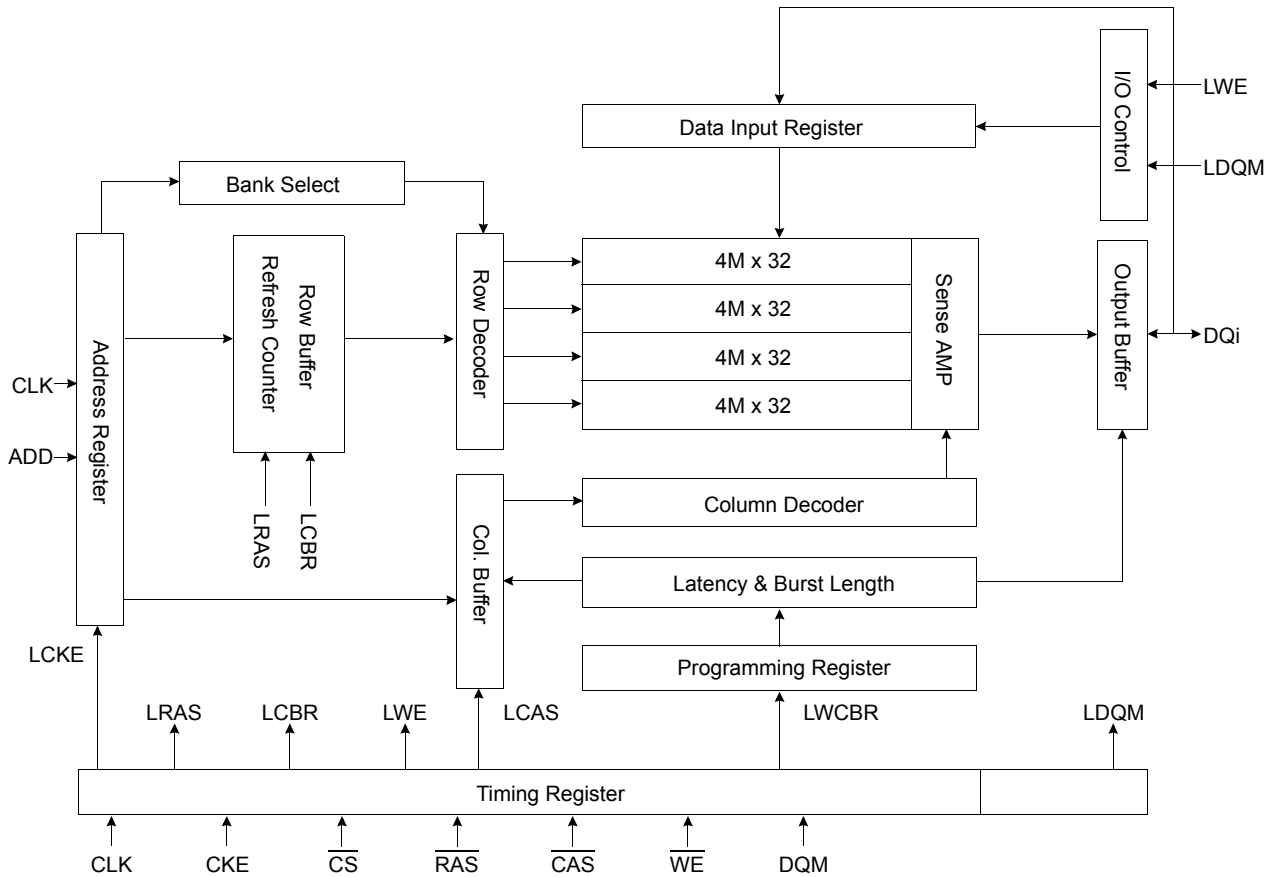
Part No.	Max Freq.	Interface	Package
K4M51323PI-HG60	166MHz(CL=3)	LVCMOS	90 FBGA (Pb Free)
K4M51323PI-HG75	133MHz(CL=3),83MHz(CL=2)		

- K4M51323PI-HG60/75 : 90FBGA (Pb Free, Halogen Free)
- K4M51323PI-HG60/75 : Low Power, Extended Temperature(-25°C ~ 85°C)

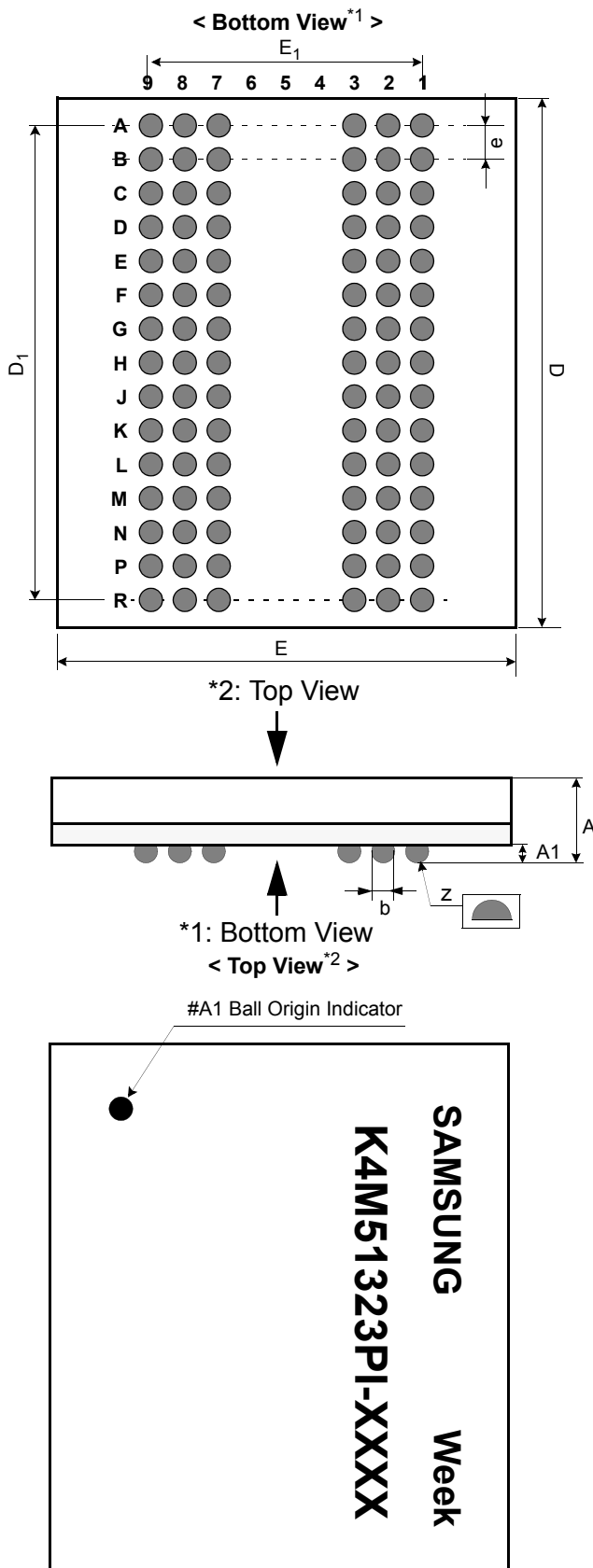
# 4.0 ADDRESS CONFIGURATION

Organization	Bank Address	Row Address	Column Address
16Mx32	BA0,BA1	A0 - A12	A0 - A8

## 5.0 FUNCTIONAL BLOCK DIAGRAM



## 6.0 PACKAGE DIMENSION AND PIN CONFIGURATION



< Top View\*2 >

90Ball(6x15) FBGA						
	1	2	3	7	8	9
A	DQ26	DQ24	Vss	Vdd	DQ23	DQ21
B	DQ28	VDDQ	VssQ	VDDQ	VssQ	DQ19
C	VssQ	DQ27	DQ25	DQ22	DQ20	VDDQ
D	VssQ	DQ29	DQ30	DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC	NC	DQ16	VssQ
F	Vss	DQM3	A3	A2	DQM2	Vdd
G	A4	A5	A6	A10	A0	A1
H	A7	A8	A12	NC	BA1	A11
J	CLK	CKE	A9	BA0	CS	RAS
K	DQM1	NC	NC	CAS	WE	DQM0
L	VDDQ	DQ8	Vss	Vdd	DQ7	VssQ
M	VssQ	DQ10	DQ9	DQ6	DQ5	VDDQ
N	VssQ	DQ12	DQ14	DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VssQ	VDDQ	VssQ	DQ4
R	DQ13	DQ15	Vss	Vdd	DQ0	DQ2

Pin Name	Pin Function
CLK	System Clock
CS	Chip Select
CKE	Clock Enable
A0 ~ A12	Address
BA0 ~ BA1	Bank Select Address
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
DQM0 ~ DQM3	Data Inputs/Outputs Mask
DQ0 ~ 31	Data Input/Output
VDD/Vss	Power Supply/Ground
VDDQ/VssQ	Data Output Power/Ground

[Unit::mm]

Symbol	Min	Typ	Max
A	-	-	1.00
A <sub>1</sub>	0.25	-	-
E	7.9	8.0	8.1
E <sub>1</sub>	-	6.40	-
D	12.9	13.0	13.1
D <sub>1</sub>	-	11.2	-
e	-	0.80	-
b	0.45	0.50	0.55
z	-	-	0.10

## 7.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 2.6	V
Voltage on V <sub>DD</sub> supply relative to V <sub>SS</sub>	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 2.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	1.0	W
Short circuit current	I <sub>OS</sub>	50	mA

**NOTE :**

- 1) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
- 2) Functional operation should be restricted to recommended operating condition.
- 3) Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## 8.0 DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V<sub>SS</sub> = 0V, T<sub>c</sub> = -25 to 85°C for Extended)

Parameter	Symbol	Min	Max	Unit	Note	
Supply voltage	V <sub>DD</sub>	1.7	1.95	V	1	
	V <sub>DDQ</sub>	1.7	1.95	V	1	
Input logic high voltage	V <sub>IH</sub>	for Add.	0.8 x V <sub>DDQ</sub>	V <sub>DDQ</sub> + 0.3	V	2
		for DQ	0.7 x V <sub>DDQ</sub>	V <sub>DDQ</sub> + 0.3	V	
Input logic low voltage	V <sub>IL</sub>	for Add.	-0.3	0.2	V	3
		for DQ	-0.3	0.3	V	
Output logic high voltage	V <sub>OH</sub>	V <sub>DDQ</sub> - 0.2	-	V	I <sub>OH</sub> = -0.1mA	
Output logic low voltage	V <sub>OL</sub>	-	0.2	V	I <sub>OL</sub> = 0.1mA	
Input leakage current	I <sub>LI</sub>	-2	2	µA	4	

**NOTE :**

- 1) Under all conditions, V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
- 2) V<sub>IH</sub> (max) = 2.2V AC. The overshoot voltage duration is ≤ 3ns.
- 3) V<sub>IL</sub> (min) = -1.0V AC. The undershoot voltage duration is ≤ 3ns.
- 4) Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
- 5) Dout is disabled, 0V ≤ V<sub>OUT</sub> ≤ V<sub>DDQ</sub>.

## 9.0 CAPACITANCE

(V<sub>DD</sub> = 1.8V, T<sub>c</sub> = 23°C, f = 100MHz, V<sub>REF</sub> = 0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
ADDs(A0 ~ A12, BA0 ~ BA1), $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	CIN1	1.5	3.0	pF	
$\overline{\text{CS}}$	CIN2	1.5	3.0	pF	
CKE	CIN3	1.5	3.0	pF	
CLK	CIN4	1.5	3.5	pF	
DQMs	CIN5	1.5	3.0	pF	
DQs(DQ0 ~ DQ31)	COU <sub>T</sub>	2.0	4.5	pF	

# 10.0 DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V<sub>SS</sub> = 0V, T<sub>c</sub> = -25 to 85°C for Extended)

Parameter	Symbol	Test Condition	Version		Unit	Note		
			-60	-75				
Operating Current (One Bank Active)	I <sub>CC1</sub>	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC(min)</sub> IO = 0 mA	65	60	mA	1		
Precharge Standby Current in power-down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = 10ns	0.3	0.3	mA			
	I <sub>CC2PS</sub>	CKE & CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞	0.3	0.3				
Precharge Standby Current in non power-down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH(min)</sub> , CS ≥ V <sub>IH(min)</sub> , t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	10	8	mA			
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH(min)</sub> , CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞ Input signals are stable	5	4				
Active Standby Current in power-down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = 10ns	3	3	mA			
	I <sub>CC3PS</sub>	CKE & CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞	2	2				
Active Standby Current in non power-down mode (One Bank Active)	I <sub>CC3N</sub>	CKE ≥ V <sub>IH(min)</sub> , CS ≥ V <sub>IH(min)</sub> , t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	12	12	mA			
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH(min)</sub> , CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞ Input signals are stable	8	8	mA			
Operating Current (Burst Mode)	I <sub>CC4</sub>	IO = 0 mA Page burst 4Banks Activated t <sub>CCD</sub> = 2CLKs	65	60	mA	1		
Refresh Current	I <sub>CC5</sub>	t <sub>ARFC</sub> ≥ t <sub>ARFC</sub>	70	70	mA	2,3		
Self Refresh Current	I <sub>CC6</sub>	CKE ≤ 0.2V	TCSR Range	Values		uA	4	
				Full Array	Typ			Max
			85°C		400			500
			70°C		250			
			45°C		150			250
			1/2 Array	15°C	140			
				85°C	300			400
				70°C	200			
				45°C	120			220
			1/4 Array	15°C	110			
				85°C	250			350
				70°C	165			
45°C	100	200						
			15°C	95				

**NOTE :**  
1) Measured with outputs open.  
2) Refresh period is 64ms.

3) ICC5 is measured under the below test condition.

Density	128Mb	256Mb	512Mb	1Gb	2Gb	Unit
t <sub>ARFC</sub>	80	80	110	140	140	ns

4) Internal TCSR can be supported.  
5) DPD(Deep Power Down) function is an optional feature, and it will be enabled upon request.  
Please contact Samsung for more information.  
6) Unless otherwise noted, input swing level is CMOS(V<sub>IH</sub> / V<sub>IL</sub> = V<sub>DDQ</sub> / V<sub>SSQ</sub>).



# 11.0 AC OPERATING TEST CONDITIONS

(VDD = 1.7 ~ 1.95 V, Tc = -25 ~ 85°C for Extended)

Parameter	Value	Unit
AC input levels (Vih/Vil)	$0.9 \times V_{DDQ} / 0.2$	V
Input timing measurement reference level	$0.5 \times V_{DDQ}$	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	$0.5 \times V_{DDQ}$	V
Output load condition	See Figure 2	

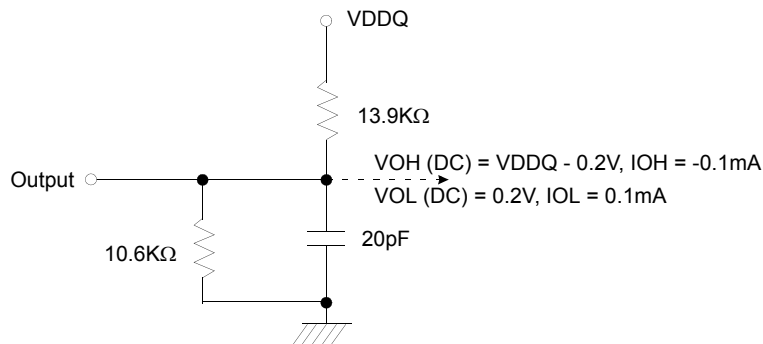


Figure 1. DC Output Load Circuit

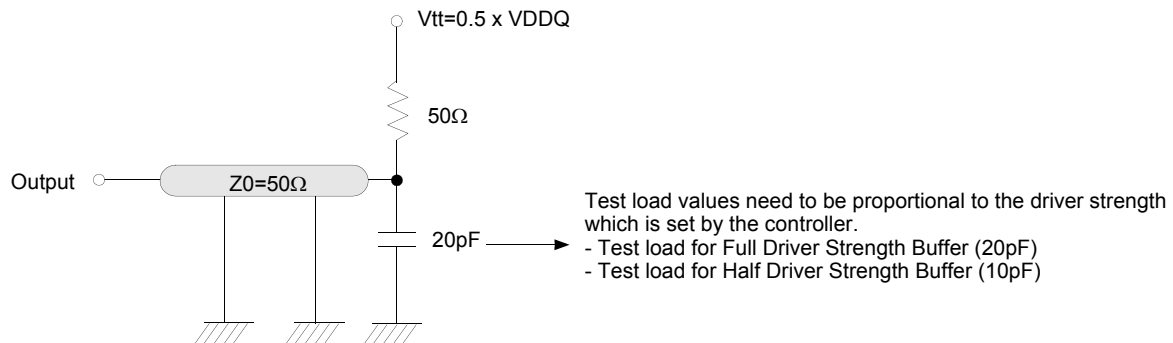


Figure 2. AC Output Load Circuit<sup>1), 2)</sup>

**NOTE :**  
1) The circuit shown above represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.

2) Based on nominal impedance at 0.5 x VDDQ. The impedance for Half(1/2) Driver Strength is designed 55ohm. And for other Driver Strength, it is designed proportionally.

## 12.0 OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version		Unit	Note
		-60	-75		
Row active to row active delay	$t_{RRD}(\text{min})$	12	15	ns	1
RAS to CAS delay	$t_{RCD}(\text{min})$	18	22.5	ns	1
Row precharge time	$t_{RP}(\text{min})$	18	22.5	ns	1
Row active time	$t_{RAS}(\text{min})$	42	50	ns	1
	$t_{RAS}(\text{max})$	100		us	
Row cycle time	$t_{RC}(\text{min})$	60	72.5	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	15		ns	2
Last data in to Active delay	$t_{DAL}(\text{min})$	$t_{RDL} + t_{RP}$		-	3
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1		CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1		CLK	2
Auto refresh cycle time	$t_{ARFC}(\text{min})$	80		ns	6
Exit self refresh to active command	$t_{SRFX}(\text{min})$	120		ns	
Col. address to col. address delay	$t_{CCD}(\text{min})$	1		CLK	4
Number of valid output data	CAS latency=3	2		ea	5
	CAS latency=2	1			

- NOTE :**
- 1) The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  - 2) Minimum delay is required to complete write.
  - 3)  $t_{DAL} = (t_{RDL}/t_{CC}) + (t_{RP}/t_{CC})$   
In case of below 33MHz ( $t_{CC} = 30\text{ns}$ ) condition, SEC could support  $t_{DAL} (=2 \cdot t_{CK})$
  - 4) All parts allow every cycle column address change.
  - 5) In case of row precharge interrupt, auto precharge and read burst stop.
  - 6) Maximum burst refresh cycle : 8

## 13.0 AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

Parameter		Symbol	-60		-75		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	$t_{CC}$	6.0	1000	7.5	1000	ns	1,2,3
	CAS latency=2		-		12			
CLK to valid output delay	CAS latency=3	$t_{SAC}$		5.4		6	ns	1,4
	CAS latency=2					9		
Output data hold time	CAS latency=3	$t_{OH}$	2.5		2.5		ns	4
	CAS latency=2		-		2.5			
CLK high pulse width		$t_{CH}$	2.5		2.5		ns	5
CLK low pulse width		$t_{CL}$	2.5		2.5		ns	5
Input setup time		$t_{SS}$	2.0		2.0		ns	5
Input hold time		$t_{SH}$	1		1		ns	5
CLK to output in Low-Z		$t_{SLZ}$	1		1		ns	4
CLK to output in Hi-Z	CAS latency=3	$t_{SHZ}$		5.4		6	ns	
	CAS latency=2			-		9		

**NOTE :**

- 1) Parameters depend on programmed CAS latency.
- 2)  $t_{CC}(\text{max})$  value is measured at 100ns.
- 3) The only time that the clock Frequency is allowed to be changed is during clock stop, power-down, self-refresh modes.
- 4) If clock rising time is longer than 1ns,  $(t_r/2-0.5)\text{ns}$  should be added to the parameter.
- 5) Assumed input rise and fall time ( $t_r$  &  $t_f$ ) = 1ns.  
If  $t_r$  &  $t_f$  is longer than 1ns, transient time compensation should be considered,  
i.e.,  $[(t_r + t_f)/2-1]\text{ns}$  should be added to the parameter.

## 14.0 SIMPLIFIED TRUTH TABLE

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12,11, A9 ~ A0	Note	
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X	X		3	
	Self Refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
	H				X							X	X
Bank Active & Row Addr.		H	X	L	L	H	H	X	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DQM		H	X					V	X		7		
No Operation Command		H	X	H	X	X	X	X	X				
				L	H	H	H						

**NOTE :**

- OP Code : Operand Code  
A0 ~ A12 & BA0 ~ BA1 : Program keys. (@MRS)
- MRS can be issued only at all banks precharge state.  
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are the same as CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.  
Partial self refresh can be issued only after setting partial self refresh mode of EMRS.
- BA0 ~ BA1 : Bank select addresses.
- During burst read or write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

## 15.0 MODE REGISTER FIELD TABLE TO PROGRAM MODES

### 15.1 Register Programmed with Normal MRS

Address	BA0 ~ BA1	A12 ~ A10/AP	A9 <sup>2)</sup>	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU <sup>1)</sup>	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

### 15.2 Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page <sup>3)</sup>	Reserved

### 15.3 Register Programmed with Extended MRS

Address	BA1	BA0	A12 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU <sup>1)</sup>			DS			RFU <sup>1)</sup>		PASR		

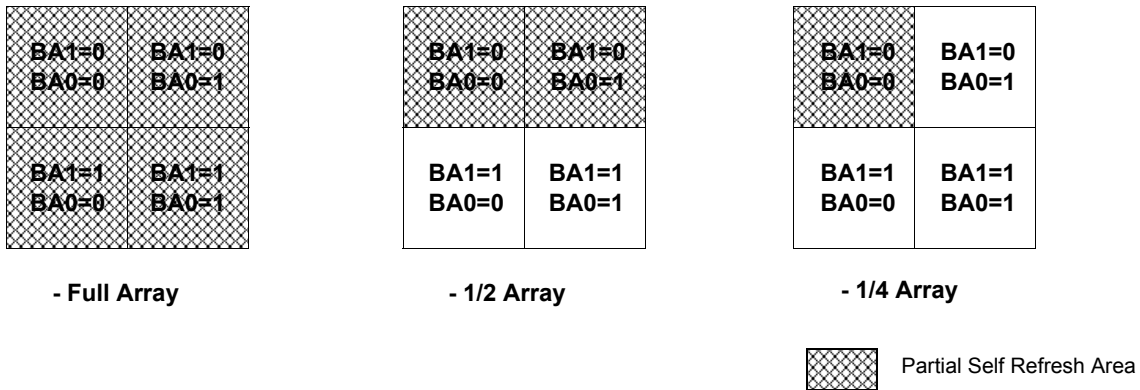
### 15.4 EMRS for PASR(Partial Array Self Ref.) & DS(Driver Strength)

Mode Select			Driver Strength					PASR					
BA1	BA0	Mode	A7	A6	A5	Driver Strength		A2	A1	A0	# of Banks		
0	0	Normal MRS	0	0	0	Full		0	0	0	Full Array		
0	1	Reserved	0	0	1	1/2		0	0	1	1/2 Array		
1	0	EMRS	0	1	0	1/4		0	1	0	1/4 Array		
1	1	Reserved	0	1	1	1/8		0	1	1	Reserved		
			1	0	0	3/4		1	0	0	Reserved		
Reserved Address			1	0	1	3/8		1	0	1	Reserved		
A12~A10/AP	A9	A8	A4	A3	1		1	0	5/8	1	1	0	Reserved
0	0	0	0	0	1		1	1	7/8	1	1	1	Reserved

- NOTE :
- 1) RFU(Reserved for future use) should stay "0" during MRS cycle.
  - 2) If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
  - 3) Full Page Length x32 : 64Mb(256) , 128Mb (256) , 256Mb (512), 512Mb (512)

### 15.4.1. Partial Array Self Refresh

1. In order to save power consumption, Mobile SDR SDRAM has PASR option.
2. Mobile SDR SDRAM supports 3 kinds of PASR in self refresh mode : Full array, 1/2 array, 1/4 array



### 15.4.2. Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, this Mobile DRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the real device temperature.
2. TCSR ranges for IDD6 shown in the table are as an example only. Max IDD6 value for 45°C, 85°C are guaranteed. Typical values for 85 °C, 70 °C, 45 °C and 15 °C are obtained from device characterization.
3. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (IDD6)						Unit
	Full Array		1/2 Array		1/4 Array		
	Typ.	Max	Typ.	Max	Typ.	Max	
85 °C	400	500	300	400	250	350	uA
70 °C	250		200		165		
45 °C	150	250	120	220	100	200	
15 °C	140		110		95		

## 16.0 POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
  - Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command for the desired operating modes after normal MRS.

The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation, all banks have to be in idle state prior to adjusting MRS and EMRS set.

# 17.0 BURST SEQUENCE

## 17.1 BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

## 17.2 BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0